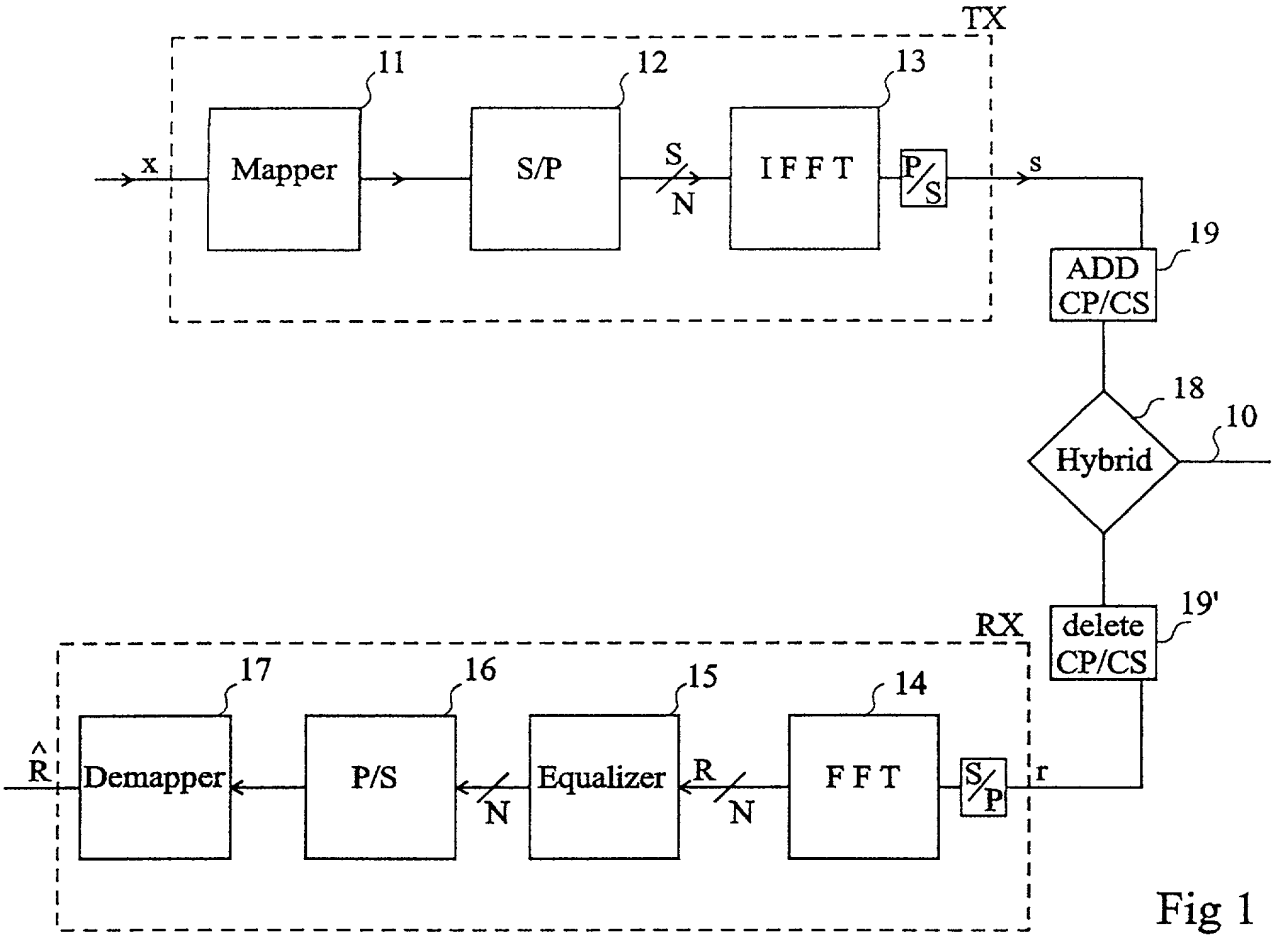

TX
11
12
13
x
Mapper
S/P
S
N
IFFT
P/S
s
19
ADD
CP/CS
18
10
Hybrid
19'
delete
CP/CS
RX
17
16
15
14
R̂
Demapper
P/S
N
Equalizer
R
N
FFT
S/P
r

Fig 1

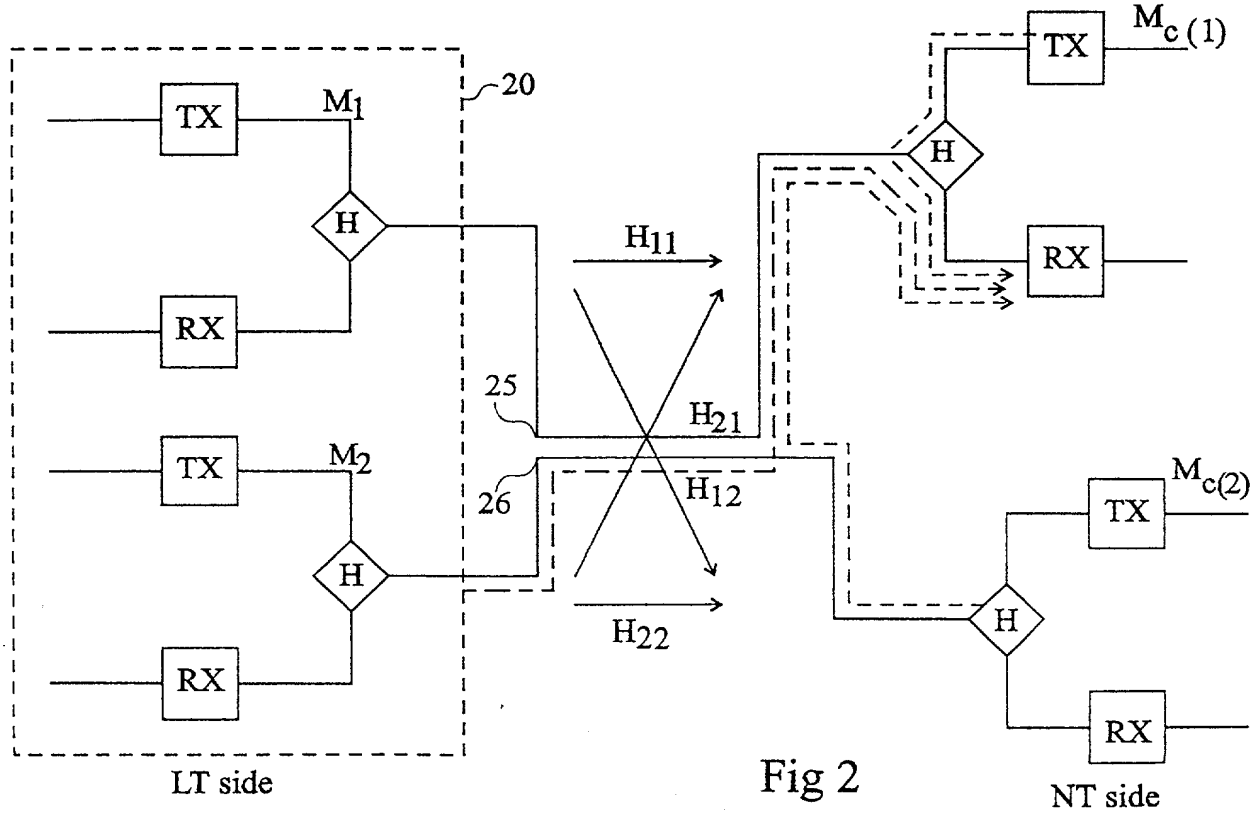

20
TX
M1
H
RX
TX
M2
H
RX
LT side
H11
H21
H12
H22
25
26
TX
Mc(1)
H
RX
TX
Mc(2)
H
RX
NT side

Fig 2

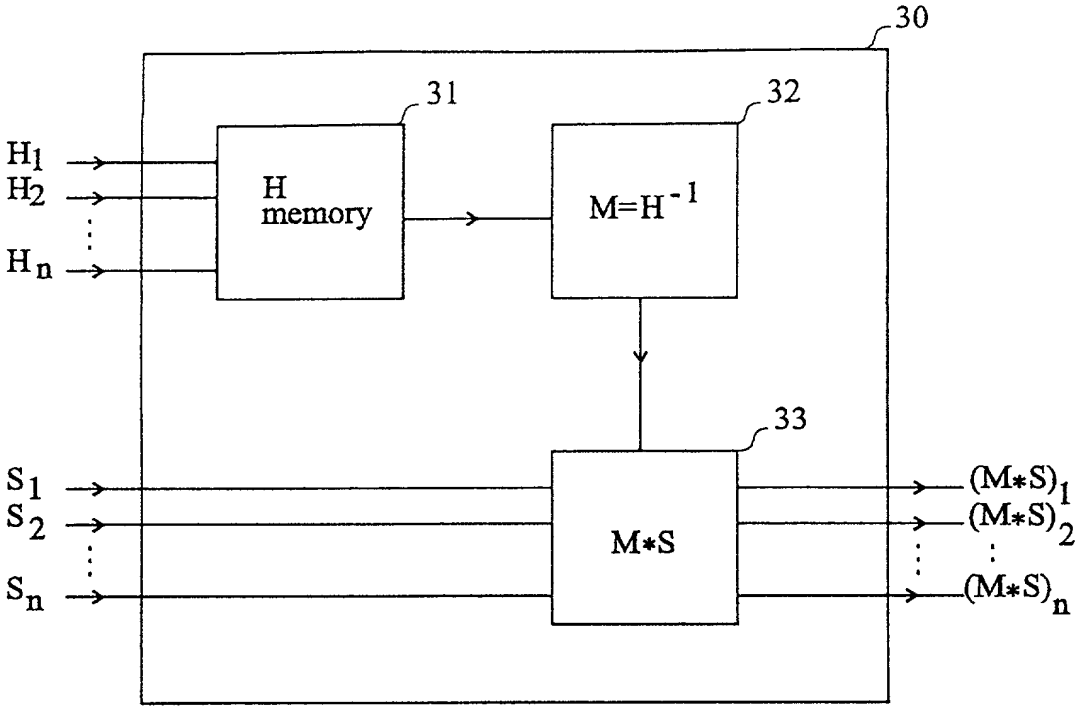

30
31
32
H1
H2
Hn
H memory
M=H-1
33
S1
S2
Sn
M*S
(M*S)1
(M*S)2
(M*S)n

Fig 3A

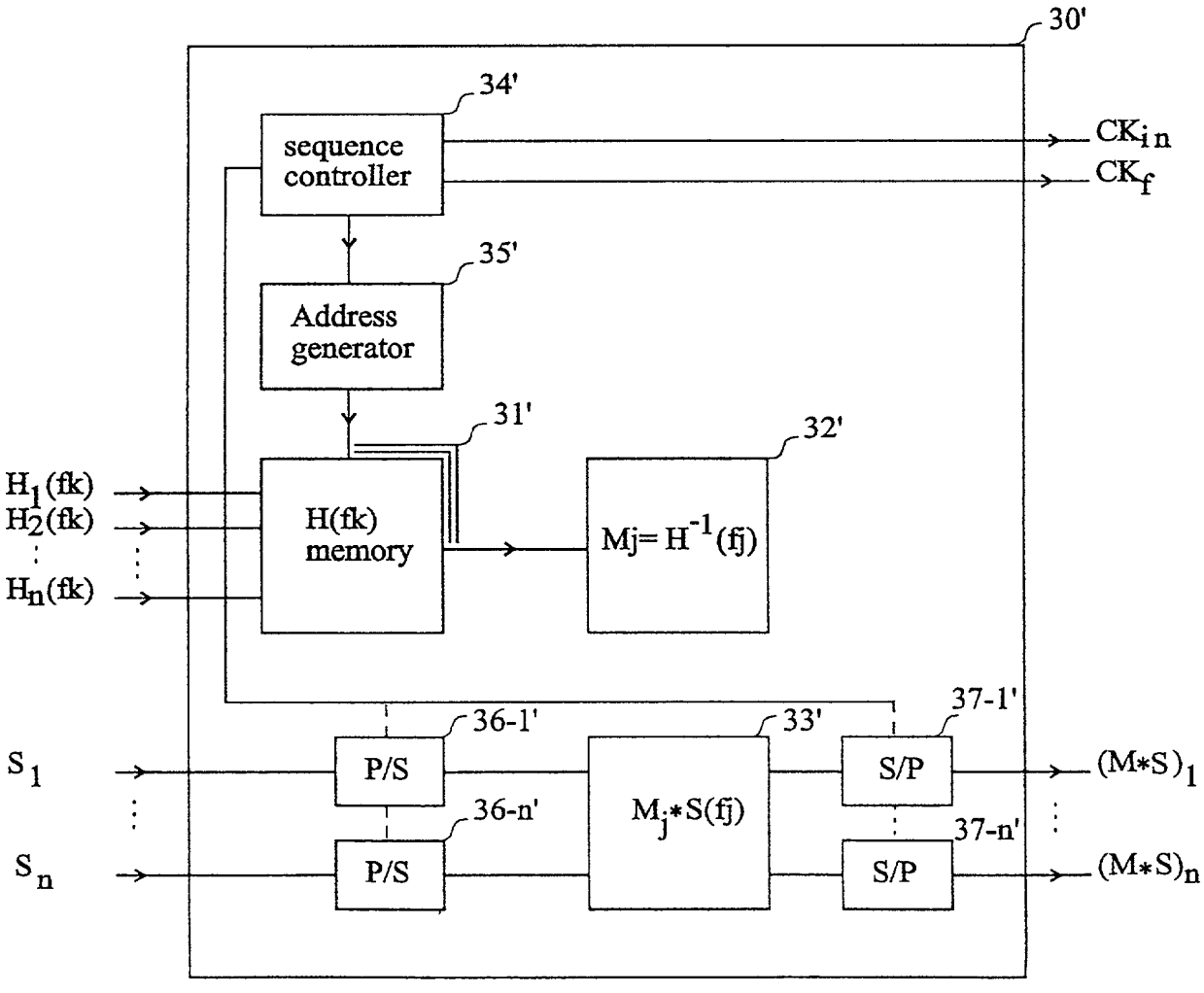

30'
34'
sequence controller
CKin
CKf
35'
Address generator
31'
32'
H1(fk)
H2(fk)
Hn(fk)
H(fk) memory
Mj= H-1(fj)
37-1'
36-1'
33'
S1
P/S
S/P
(M*S)1
Mj*S(fj)
36-n'
37-n'
Sn
P/S
S/P
(M*S)n

Fig 3B

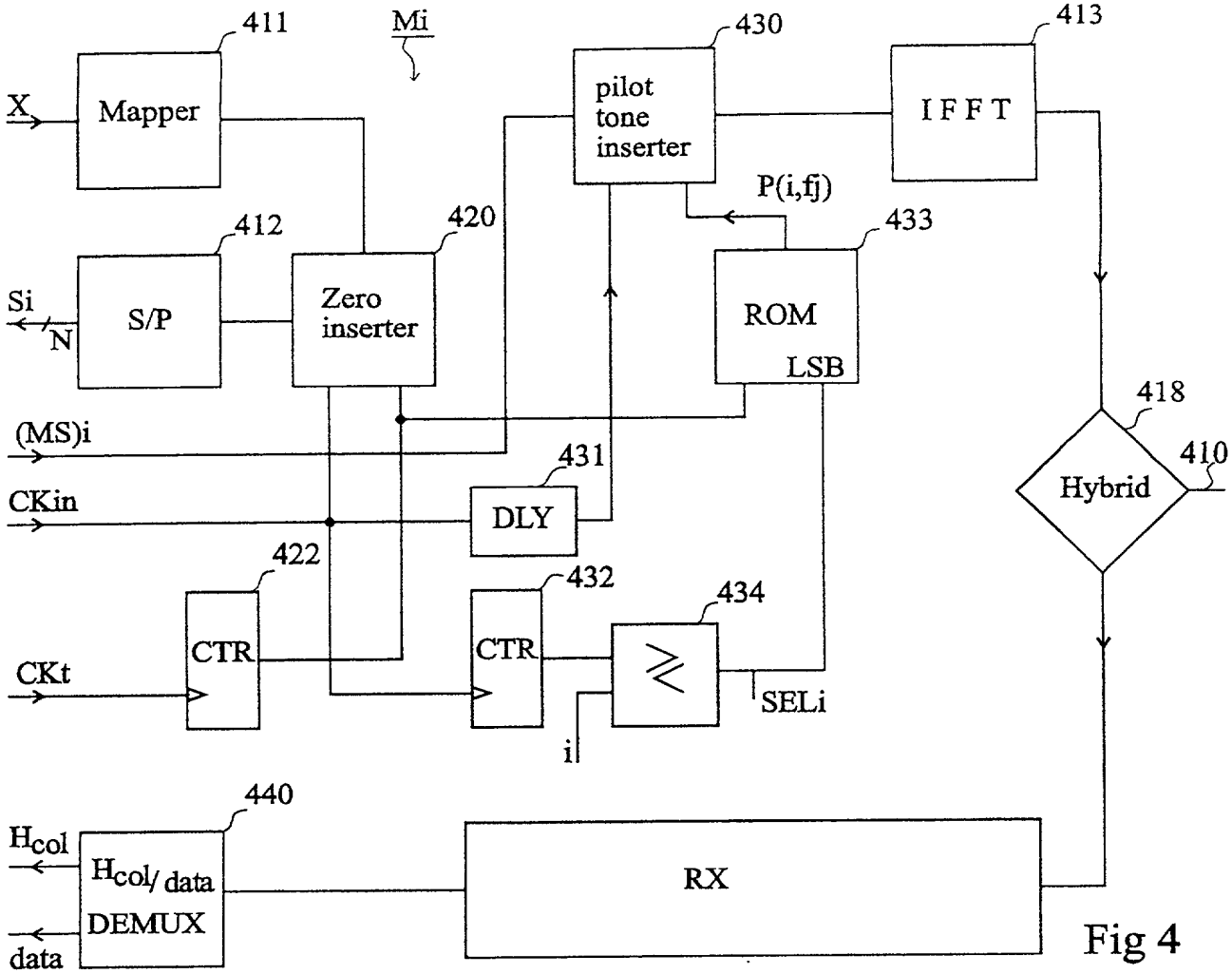

411
Mi
430
413
X
Mapper
pilot tone inserter
IFFT
P(i,fj)
412
420
433
Si
N
S/P
Zero inserter
ROM
LSB
418
(MS)i
431
410
Hybrid
CKin
DLY
422
432
434
CTR
CTR
CKt
SELi
i
440
Hcol
Hcol/ data
DEMUX
data
RX

Fig 4

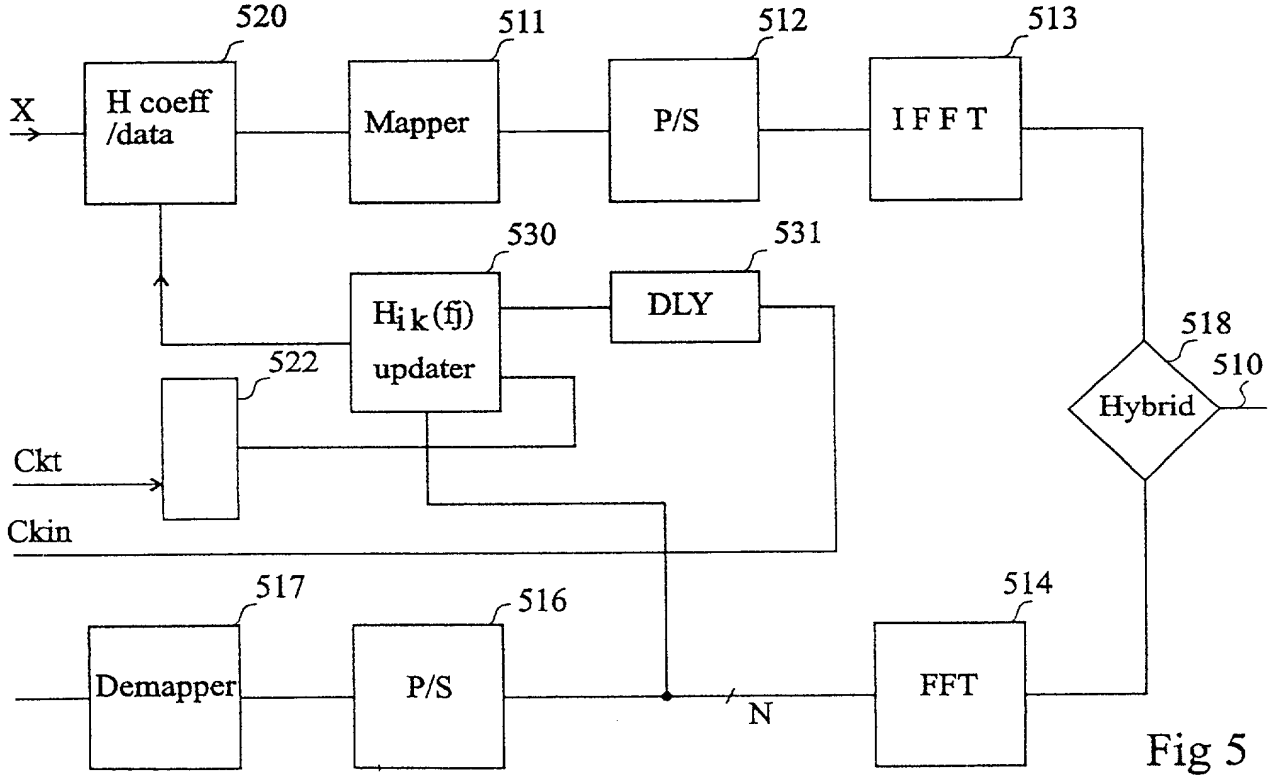

520
511
512
513
X
H coeff /data
Mapper
P/S
IFFT
530
531
Hi k(fj) updater
DLY
518
522
510
Hybrid
Ckt
Ckin
517
516
514
Demapper
P/S
N
FFT

Fig 5

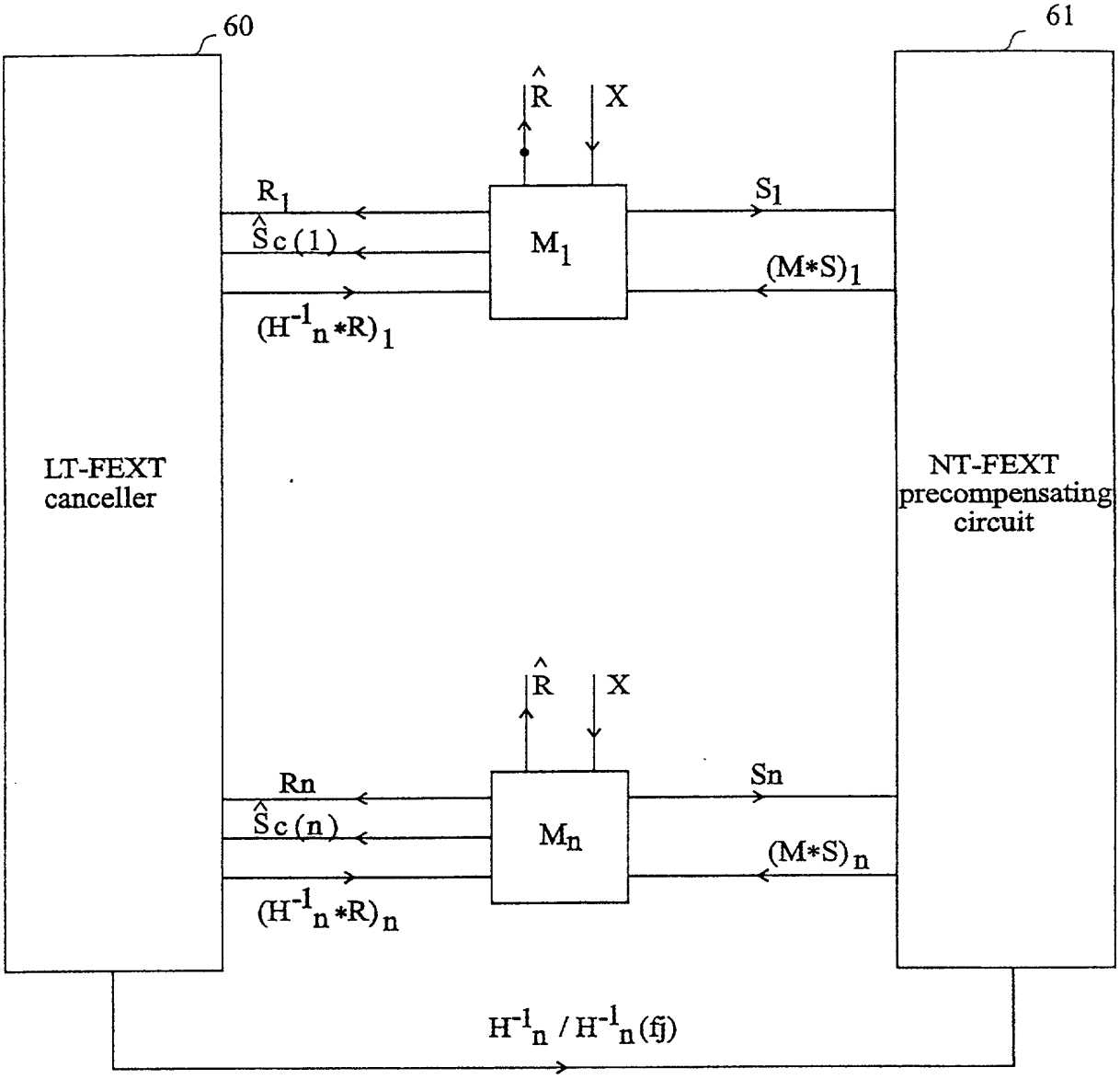

60
61
$\hat{R}$
X
R_1
$\hat{S}c(1)$
$(H^{-1}{}_n * R)_1$
M_1
S_1
$(M*S)_1$
LT-FEXT canceller
NT-FEXT precompensating circuit
$\hat{R}$
X
Rn
$\hat{S}c(n)$
$(H^{-1}{}_n * R)_n$
M_n
Sn
$(M*S)_n$
$H^{-1}{}_n$ / $H^{-1}{}_n(fj)$

Fig 6